SIT-1579

Compact MIL-STD-1553/1760 Transceiver Module

Part Numbers

SIT-1579	-40° C to +85° C
SIT-1579-ET	-55° C to +125° C

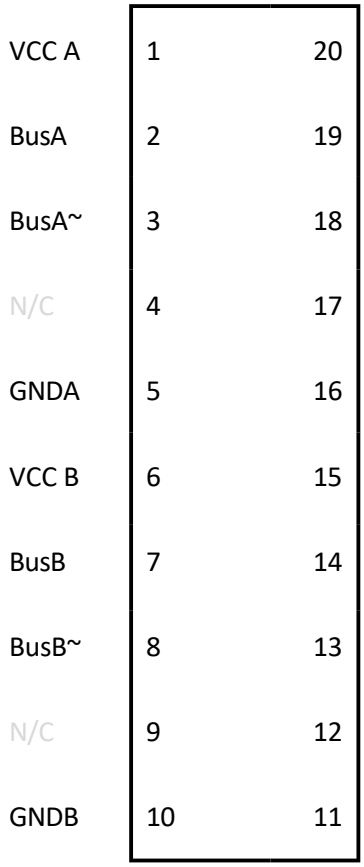
SIT-1579 dual MIL-STD-1553 Transceiver

The SIT-1579 is a MIL-STD-1553/ transceiver module based on the SIT-1579 transceiver design with discrete components assembled on a daughter board that is pin compatible with HOLT's HI1579 monolithic transceiver. The SIT-1579 interfaces between the digital domain signals from the FPGA 3v3 signals and the MIL-STD-1553 transformer. By using discrete components, the SIT-1579 uses state of art power switching devices which reduce the power dissipation to a record of 0.25W when transmitting 100% of the time. No special heat dissipation pads are needed.

SIT-1579 is delivered in 20 PIN QFN PCB that fits the PCB foot print of the HI-1579 SOIC-20.

SIT-1579 presents a breakthrough in transceiver design in a number of ways. In terms of cost, standard 1553 COTS transceivers require special manual & costly symmetry alignments for every component going off the fabrication line. SIT-1579 on the other hand does not have any such alignment during fabrication, but rather online, once the power is engaged, and during each and every transmission. This dynamic alignment balances and eliminates the symmetry issues that are common with 1553 transceivers resulting in higher quality signaling at a lower cost. A typical 1553 COTS transceiver comprises of a digital part and an analogue part. The SIT-1579 only contains the analogue parts, and the digital is embedded inside the FPGA. The FPGA digital part of the transceiver manages the symmetry alignment in addition to noise filtering and short detection.
SIT-1579 is designed to work with the BRM1553D FPGA IP as it contains the digital alignment logic and is not a drop in replacement for the HI-1579. It is intended for Sital customers that use Sital Technology's 1553 IP, and the HI-1579 transceiver.

- MIL-STD-1553A and B, MIL-STD-1760
- 3.3V supply
- Industry standard pin configuration
- Works with the following IP Cores:
  - BRM1553D
  - DO254BRM1553D
  - BRM1553FE
  - BRM1553PCI
  - BRM1553SPI
  - BRM1553D-SnS



20 pin QFN PCB
fits
SOIC-20 package

Absolute Maximum Rating	
Supply Voltage(VCC)	-0.3V … +3.5V
Logic Input	-0.3V … +VCC
Receiver Voltage	30 V p-p
Driver Current	700 mA
Reflow Solder	245 °C
Junction temperature	175 °C
Storage temperature	-65°C…+150 °C

Pinout description

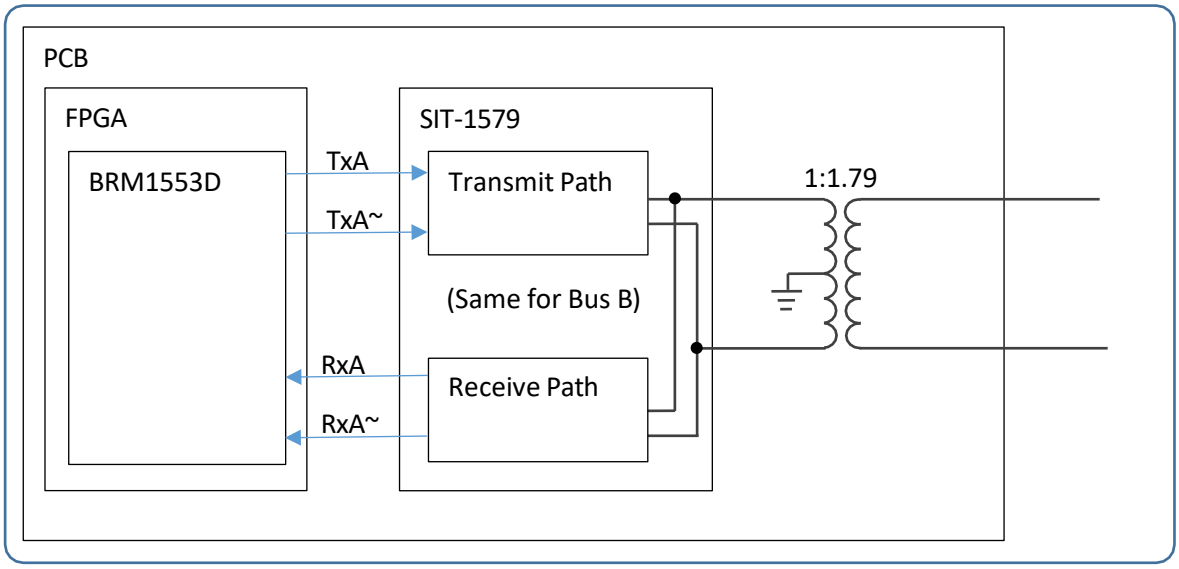
Pin Number	Symbol	Description
1	VCC A	3.3 Volts input power supply for Channel A only.
2	BusA	Transformer positive side connection
3	BusA~	Transformer negative side connection
4	N/C	No Connection inside. Might be wired to Rx Enable.
5	GNDA	Ground of channel A only.
6	VCC B	3.3 Volts input power supply for Channel B only.
7	BusB	Transformer positive side connection
8	BusB~	Transformer negative side connection
9	N/C	No Connection inside. Might be wired to Rx Enable.
10	GNDB	Ground of channel B only.
11	RxB~	Output of inverted bus to FPGA.
12	RxB	Output of non-inverted bus to FPGA.
13	N/C	No Connection inside. Might be wired to Tx Inhibit.
14	TxB	Input of non-inverted Bus B transmit signal.
15	TxB~	Input of inverted Bus B transmit signal.
16	RxA~	Output of inverted bus to FPGA.
17	RxA	Output of non-inverted bus to FPGA.
18	N/C	No Connection inside. Might be wired to Tx Inhibit.
19	TxA	Input of non-inverted Bus transmit signal.
20	TxA~	Input of inverted Bus transmit signal.

DC electrical characteristics

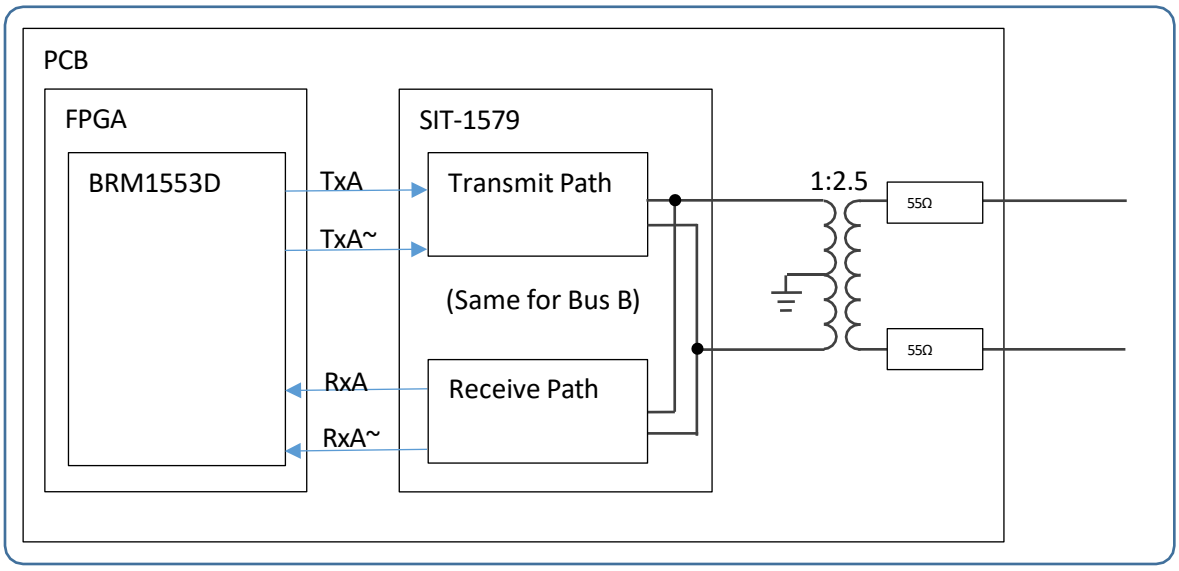
Parameter	Symbol	Condition	Min	Typical	Max	Units
Operating Voltage	VCC	A or B	3.15	3.30	3.50	Volts
Total Supply Current	ICC1	No Transmission		10	15	mA
	ICC2	50% Transmission		250	270	mA
	ICC3	100% Transmission		500	550	mA
Power dissipation	P1	No Transmission		30	60	mW
	P2	100% Transmission		250	280	mW
FPGA IO setting for Tx and Rx	IO	LVCMOS33 / LVTTL33	-0.3	3.3	3.5	V
Output Voltage (transformer coupled)	Vout	70Ω load @ 3.30V	18.2	18.6	19.5	V
Input Voltage	Vdiff	At receiver inputs			12	V
Operating Temperature	Ta	Industrial (SIT-1579)	-40		85	°C
	Tm	MIL-Part (SIT-1579-ET)	-55		125	°C

Block Diagram

Transformer coupling to coupler



Direct coupling to bus



Functional description

Transmit Path

The FPGA IP provides two transmit signals Tx and Tx~ for bus A and bus B. As opposed to COTS transceivers, the Tx Inhibit signal is not required for the transceiver since the transmission inhibit is done in the IP inputs. If the transmission is inhibited by an external line it will enter the IP as the inhibit A and B inputs and would mute the Tx and Tx~ signals.

Tx and Tx~ should be connected directly to the FPGA pins, no buffers should be used, since HI-Z state is used during normal operation. Tx and Tx~ logic levels are 0V for low logic level and 3.3V for the high logic level.

The Digital part of the transmit path inside the FPGA shapes the Tx and Tx~ signals such that the SIT-1579 would transmit a properly shaped trapezoid signal with rising and falling edges of about 125 ns.

In the case that the bus is shorted, or even the primary transformer is shorted, the SIT-1579 has a built in protection against overcurrent which would limit the source current to 700 mA and prevent overheating. Once the short is gone, the transmit path returns to normal operation.

Receive Path

The receiver circuit inside SIT-1579 contains an analogue filter that reduces noise, determines the minimum detected signal which is half way between the standard's minimum required and the standard's maximum no detection limit, i.e., 550 mV p-p for transformer coupled.

Symmetry alignment

Both transmit and receive paths cooperate in the effort to keep the MIL-STD-1553 signal symmetric. Traditional COTS transceivers are balanced for symmetry during the final stages of fabrication, a costly process resulting in expensive transceiver offerings with known performance symmetry issues. This process is required since the push pull switching circuits for the two transformer pins, Bus and Bus~, are never identical and tend to charge the bus with the difference between the switches. In COTS transceivers this compensation process is mandatory and significantly contribute to component cost. SIT-1579 uses a calibration loop that measures the symmetry fault in the receive path, and reshapes the Tx and Tx~ signals going to the transmit path. The advantage of this calibration is that it compensates for the transceiver components symmetry issues if exist, but also to overcome possible PCB wiring or transformer symmetry issues, and thus assures that the transmitted signal is perfectly symmetric. The calibration is done from the first transmission to the very last one. The real-time symmetry alignment is a novel approach allowing for higher signal symmetry reliability, easier design and development and at lower costs.

Mechanical Shape

QFN package fits SOIC - 20