MIL-STD-1553 Terminal

OCTAVA

For 1553 Remote Terminal, Bus Controller and Monitor applications

Compact, Robust, Reliable
MIL-STD-Products

Specifications

Compatibility
- MIL-STD-1553B Notice 2
- DDC® MiniACE® 72 Pin Gull-Lead BU-65178, BU-61588, BU-65179, BU-61688 and BU-61689 pinout and software

Available Configurations
- **OCT-61688**
  - BC/RT/MT
  - 12/16MHz Clock
  - 64K x 16 bits RAM
- **OCT-61588**
  - BC/RT/MT
  - 12/16MHz Clock
  - 4K x 16 bits RAM
- **OCT-65179**
  - RT/RT_BOOT
  - 10/12/16/20MHz Clock
  - 4K x 16 bits RAM
- **OCT-65178**
  - RT Only
  - 12/16MHz Clock
  - 4K x 16 bits RAM
- **OCT-61689**
  - BC/RT/MT
  - 10/20MHz Clock
  - 64K x 16 bits RAM
- **All devices**
  - Temperature range: -40^{0}C - +85^{0}C Industrial
  - Power: 5VDC or 3.3VDC

More 1553 products from Sital
- *MIL-STD-1553 IP Cores for FPGAs.*
- *MIL-STD-1553 Discrete Components Transceiver*
- *MIL-STD-1553 Obsolete Replacement Services*
- *Mil-Std-1553 Testers*

Key Features and Benefits

- Fully integrated MIL-STD-1553B Notice 2 compliant terminals
- Second source for DDC® MiniACE® devices
- 5V or 3.3V operation
- Flexible Processor/Memory interface
- Bootable RT option required for MIL-STD-1760
- Very fast access 4Kx16, 8Kx16 or 64Kx16 shared RAM
- Automatic BC Retry
- Programmable BC Gap Times
- Programmable BC Message Rate
- Programmable illegalization
- Simultaneous RT/MT mode
- Operates from 10, 12, 16 or 20 Mhz
- 72 Pins PQFP One-Square-Inch package

The OCTAVA™ family of Mil-Std-1553 devices integrate Mil-Std-1553B protocol engine, a dual 5-volt transceiver, memory management, processor interface logic, and 4K or 64K words of RAM in a 72 Pin Plastic Quad Flat Pack (PQFP) package.

The OCT-XXXXX components are pin-to-pin replacement devices for the corresponding DDC® BU-XXXXX. These replacements offer software and electrical compatible solution. For example, a board designed to operate with the DDC® BU-65178 and BU-61688 can work seamlessly with OCT-65178 and OCT-61688 without hardware or software changes*.

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Back-End Interface

The OCTAVA™ family contains internal address latches and bidirectional data buffers to provide a direct interface to a host processor bus. The memory management scheme for RT mode provides three data structures for buffering incoming and outgoing data. Combined with OCTAVA's extensive interrupt capability, these structures serve to ensure data consistency while off-loading the host processor. OCTAVA devices can optionally boot-up as a RT with the Busy bit set for 1760 applications. OCTAVA BC mode implements several features aimed at providing an efficient real-time software interface to the host processor including automatic retries, programmable inter-message gap times or message rate, automatic frame repetition, and flexible interrupt generation.

Package Information
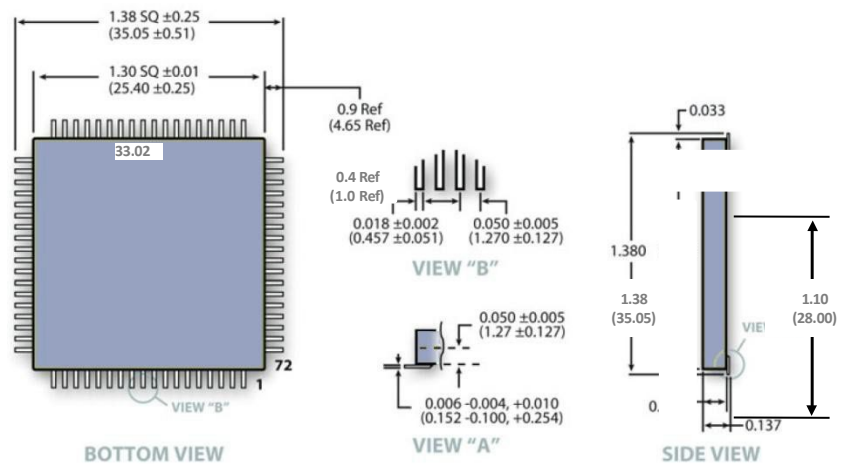
Notes:
1) Dimensions are in inches (mm)

Interface to the 1553 Bus

OCTAVA components require a coupling transformer with a turns ratio of 1: 2.5 for Direct Coupling, and a turns ratio of 1: 1.79 for Transformer Coupling to the Mil-Std- 1553 Bus.

The center tap on the OCTAVA side of the coupling transformer must be grounded. The center tap on the bus side of the coupling transformer should be left floating.
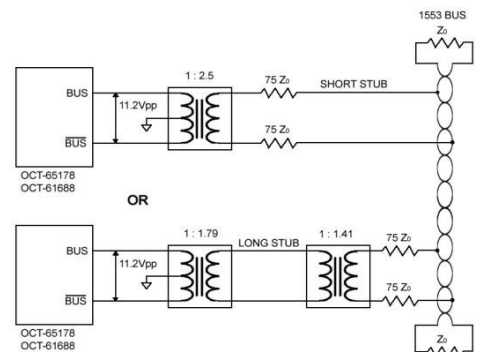
About Sital Technology

Founded in 1993, Sital Technology is a leading provider of IP cores and products for Mil-Std-1553.

SITAL Technology's key quality resource is its creative, talented and professional staff. Our engineers are veterans of the Israeli Air Force, who served in the technical units of the F-16 avionics systems. They gained knowledge and experience with the MIL-STD-1553 standard from the bottom up, both as design engineers for MIL-STD-1553 components and as technicians working on the aircrafts.

Among our many customers you can find NASA, ESA, Thales, Orbital Science Corp., Elbit, Rafael, Israeli Aerospace Industries (IAI), Astronautics, Israeli Ministry of Defense, Elta, Honeywell, BAE Systems and many others.

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