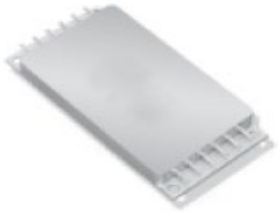
AFL50XXD Series
50V Input, Dual Output

Part Numbers: AFL5005D, AFL5012D, AFL5015D



Advanced Product Brief

The AFL Series of DC/DC converters feature high power density with no derating over the full military temperature range. This series is offered as part of a complete family of converters providing single and dual output voltages and operating from nominal +28V or +270V inputs with output power ranging from 80W to 120W. For applications requiring higher output power, individual converters can be operated in parallel. The internal current sharing circuits assure equal current distribution among the paralleled converters. This series incorporates our proprietary magnetic pulse feedback technology providing optimum dynamic line and load regulation response. This feedback system samples the output voltage at the pulse width modulator fixed clock frequency, nominally 550KHz. Multiple converters can be synchronized to a system clock in the 500KHz to700KHz range or to the synchronization output of one converter. Undervoltage lockout, primary and secondary referenced inhibit, soft-start and load fault protection are provided on all models.

These converters are hermetically packaged in two enclosure variations, utilizing copper core pins to minimize resistive DC losses. Three lead styles are available, each fabricated with our rugged ceramic lead to-package seal assuring long term hermeticity in the most-harsh environments.

Manufactured in a facility fully qualified to MIL-PRF-38534, these converters are fabricated utilizing DSCC qualified processes. For available screening options, refer to device screening table in the data sheet. Variations in electrical, mechanical and screening can be accommodated.

Features

- 30V to 80V Input Range
- ±5V, ±12V, and ±15V Outputs Available
- High Power Density - up to 70W/in^3
- Up to 100W Output Power
- Parallel Operation with Power Sharing
- Low Profile (0.380") Seam Welded Package
- Ceramic Feed-Thru Copper Core Pins
- High Efficiency - to 85%
- Continuous Short Circuit and Overload Protection
- Output Voltage Trim
- Primary and Secondary Referenced Inhibit Functions
- Line Rejection > 40dB - DC to 50KHz
- External Synchronization Port
- Fault Tolerant Design
- Single Output Versions Available
- Standard Microcircuit Drawing Available

Revision History

Revision	Description	Release Date
1.0	AFL50XXD Micross Datasheet	11/21/2024

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1.0 Specifications

Table 1. Absolute Maximum Ratings	
Input Voltage	-0.5V to +50VDC
Soldering Temperature	300°C for 10 seconds
Operating Case Temperature	-55°C to +125°C
Storage Case Temperature	-65°C to +135°C

Table 2. Static Characteristics

-55°C < T_{CASE} ≤ +125°C, 30V ≤ V_{IN} ≤ 80V Unless Otherwise Specified

Parameter	Group A Subgroups	Test Conditions	Min	Nom	Max	Unit
Input Voltage		Note 6	160	270	400	V
Output Voltage		V_{IN} = 50V, 100% Load				
AFL5005D	1	Positive Output	4.95	5.00	5.05	
	1	Negative Output	-5.05	-5.00	-4.95	
AFL5012D	1	Positive Output	11.88	12.00	12.12	
	1	Negative Output	-12.12	-12.00	-11.88	
AFL5015D	1	Positive Output	14.85	15.00	15.15	
	1	Negative Output	-15.15	-15.00	-14.85	V
AFL5005D	2,3	Positive Output	4.90		5.10	
	2,3	Negative Output	-5.10		-4.90	
AFL5012D	2,3	Positive Output	11.76		12.24	
	2,3	Negative Output	-12.24		-11.76	
AFL5015D	2,3	Positive Output	14.70		15.30	
	2,3	Negative Output	-15.30		-14.70	
Output Current		V_{IN} = 30, 50, 80V. Notes 6,11				
AFL5005D		Either Output			12.8	
AFL5012D		Either Output			6.4	A
AFL5015D		Either Output			5.3	
Output Power		Total of Both Outputs. Notes 6,11				
AFL5005D					80	W

Table 2. Static Characteristics Cont.						
-55°C < T_{CASE} ≤ +125°C, 30V ≤ V_{IN} ≤ 80V Unless Otherwise Specified						
Parameter	**Group A Subgroups**	**Test Conditions**	**Min**	**Nom**	**Max**	**Unit**
Output Power		Total of Both Outputs. Notes 6,11				
AFL5012D					96	W
AFL5015D					100	
Maximum Capacitive Load		Each Output. Note 1	10,000			µF
Output Voltage Temperature Coefficient		V_{IN} = 50V, 100% Load. Notes 1,6	-0.015		+0.015	%/°C
Output Voltage Regulation		Note 10				
Line	1,2,3	No Load, 50% Load, 100% Load	-0.5		+0.5	
Load	1,2,3	V_{IN} = 30, 50, 80V	-1.0		+1.0	
Cross		V_{IN} = 30, 50, 80V. Note 12				
AFL5005D	1,2,3	Positive Output	-1.0		+1.0	
		Negative Output	-8.0		+8.0	%
AFL5012D	1,2,3	Positive Output	-1.0		+1.0	
		Negative Output	-5.0		+5.0	
AFL5015D	1,2,3	Positive Output	-1.0		+1.0	
		Negative Output	-5.0		+5.0	
Output Ripple Voltage		V_{IN} = 30, 50, 80V, 100% Load BW = 10MHz				
AFL5005D	1,2,3				60	
AFL5012D	1,2,3				80	mVpp
AFL5015D	1,2,3				80	
Input Current		V_{IN} = 50V				
No Load	1	I_{OUT} = 0			50	
	2,3				60	mA
Inhibit 1	1,2,3	Pin 4 Shortened to Pin 2			5.0	
Inhibit 2	1,2,3	Pin 12 Shortened to Pin 8			5.0	
Input Ripple Current		V_{IN} = 50V, 100% Load				
AFL5005D	1,2,3				60	mApp

Table 2. Static Characteristics Cont.						
-55°C < T_{CASE} ≤ +125°C, 30V ≤ V_{IN} ≤ 80V Unless Otherwise Specified						
Parameter	**Group A Subgroups**	**Test Conditions**	**Min**	**Nom**	**Max**	**Unit**
Input Ripple Current		V_{IN} = 50V, 100% Load				
AFL5012D	1,2,3				60	mApp
AFL5015D	1,2,3				60	
Current Limit Point		V_{OUT} = 90% V_{NOM}, Current split equally on positive and negative outputs. Note 5				
Expressed as Percentage of Full Rated Load	1		115		125	%
	2		105		115	
	3		125		140	
Load Fault Power Dissipation		V_{IN} = 50V				
Overload or Short Circuit	1,2,3				32	W
Efficiency		V_{IN} = 50V, 100% Load				
AFL5005D	1,2,3		78	81		
AFL5012D	1,2,3		80	84		%
AFL5015D	1,2,3		81	85		
Enable Inputs (Inhibit Function)						
Converter Off		Logical Low on Pin 4 or Pin 12	-0.5		0.8	V
Sink Current		Note 1			100	µA
Converter On		Logical High on Pin 4 & 12. Note 9	2.0		50	V
Sink Current		Note 1			100	µA
Switching Frequency	1,2,3		500	550	600	KHz
Synchronization Input						
Frequency Range	1,2,3		500		700	KHz
Pulse Amplitude, Hi	1,2,3		2.0		10	V
Pulse Amplitude, Lo	1,2,3		-0.5		0.8	V
Pulse Rise Time		Note 1			100	ns
Pulse Duty Cycle		Note 1	20		80	%

Table 2. Static Characteristics Cont.						
-55°C < T_{CASE} ≤ +125°C, 30V ≤ V_{IN} ≤ 80V Unless Otherwise Specified						
Parameter	**Group A Subgroups**	**Test Conditions**	**Min**	**Nom**	**Max**	**Unit**
Isolation	1	Input Output or Any Pin to Case (except Pin 3). Test @ 500VDC	100			MΩ
Device Weight		Slight Variations with Case Style		85		g
MTBF		MIL-HDBK-217F, AIF at T_C = 70°C	300			KHrs

Table 3. Dynamic Characteristics							
-55°C ≤ T_{CASE} ≤ +125°C, V_{IN} = 50V Unless Otherwise Specified							
Parameter		**Group A Subgroups**	**Test Conditions**		**Min**	**Nom**	**Max**	**Unit**
Load Transient Response			Notes 2,8					
AFL5005D	Amplitude	4,5,6	Load Step	50% ↔ 100%	-450		450	mV
	Recovery	4,5,6					200	µs
Either Output	Amplitude	4,5,6	Load Step	10% ↔ 50%	-450		450	mV
	Recovery	4,5,6		10% ↔ 50%			200	µs
				50% ↔ 10%			400	µs
AFL5012D	Amplitude	4,5,6	Load Step	50% ↔ 100%	-750		750	mV
	Recovery	4,5,6					200	µs
Either Output	Amplitude	4,5,6	Load Step	10% ↔ 50%	-750		750	mV
	Recovery	4,5,6		10% ↔ 50%			200	µs
				50% ↔ 10%			400	µs
AFL5015D	Amplitude	4,5,6	Load Step	50% ↔ 100%	-750		750	mV
	Recovery	4,5,6					200	µs
Either Output	Amplitude	4,5,6	Load Step	10% ↔ 50%	-750		750	mV
	Recovery	4,5,6		10% ↔ 50%			200	µs
				50% ↔ 10%			400	µs
Line Transient Response			Notes 1,2,3					
	Amplitude		V_{IN} Step = 30 ↔ 80V		-500		500	mV
	Recovery						500	µs

Table 3. Dynamic Characteristics Cont.						
-55°C ≤ T_{CASE} ≤ +125°C, V_{IN} = 50V Unless Otherwise Specified						
Parameter	**Group A Subgroups**	**Test Conditions**	**Min**	**Nom**	**Max**	**Unit**
Turn-On Characteristics		Note 4				
Overshoot	4,5,6	Enable 1,2 on. (Pins 4, 12 high or open)			250	mV
Delay	4,5,6		50	75	120	ms
Load Fault Recovery		Same as Turn-On Characteristics				
Line Rejection		MIL-STD-461, CS101, 30Hz to 50KHz – Note 1	40	50		dB

Notes to Specifications:

1. Parameters not 100% tested but are guaranteed to the limits specified in the table.
2. Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1.0% of V_{OUT} at 50% load.
3. Line transient transition time ≥ 100µs.
4. Turn-on delay is measured with an input voltage rise time of between 100V and 500V per millisecond.
5. Current limit point is that condition of excess load causing output voltage to drop to 90% of nominal.
6. Parameter verified as part of another test.
7. All electrical tests are performed with the remote sense leads connected to the output leads at the load.
8. Load transient transition time ≥ 10µs.
9. Enable inputs internally pulled high. Nominal open circuit voltage ≈ 4.0VDC.
10. Load current split equally between $+V_{OUT}$ and $-V_{OUT}$.
11. Output load must be distributed so that a minimum of 20% of the total output power is being provided by one of the outputs.
12. Cross regulation measured with load on tested output at 20% of maximum load while changing the load on other output from 20% to 80%.

2.0 Block Diagram

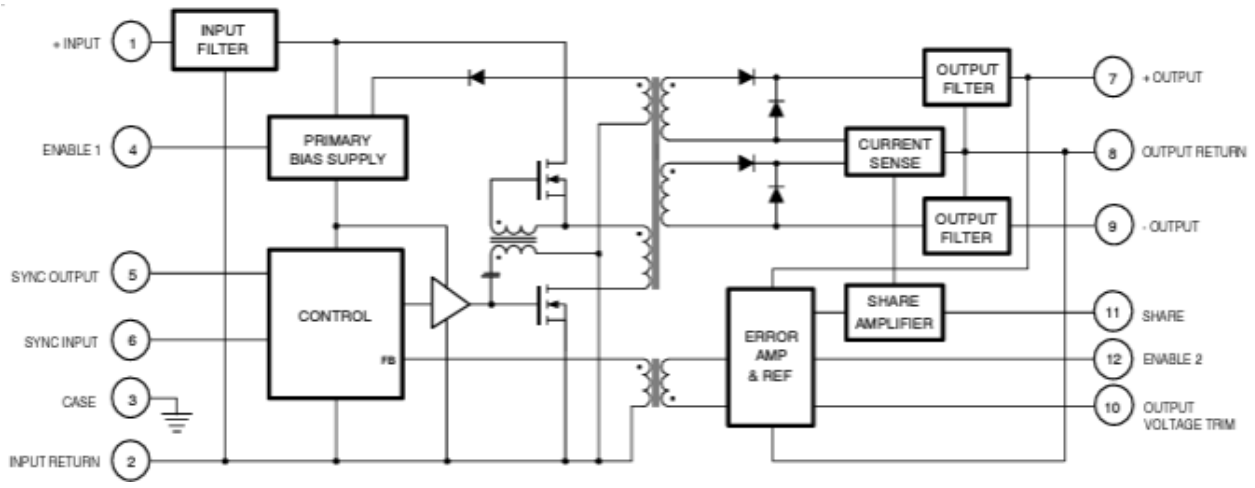

Figure 1. AFL Dual Output

3.0 Circuit Operation and Application Information

The AFL series of converters employ a forward switched mode converter topology. (refer to Figure 1.) Operation of the device is initiated when a DC voltage whose magnitude is within the specified input limits is applied between pins 1 and 2. If pins 4 and 12 are enabled (at a logical 1 or open) the primary bias supply will begin generating a regulated housekeeping voltage bringing the circuitry on the primary side of the converter to life. Two power MOSFETs used to chop the DC input voltage into a high frequency square wave, apply this chopped voltage to the power transformer. As this switching is initiated, a voltage is impressed on a second winding of the power transformer which is then rectified and applied to the primary bias supply. When this occurs, the input voltage is excluded from the bias voltage generator and the primary bias voltage becomes internally generated.

The switched voltage impressed on the secondary output transformer windings is rectified and filtered to provide the positive and negative converter output voltages. An error amplifier on the secondary side compares the positive output voltage to a precision reference and generates an error signal proportional to the difference. This error signal is magnetically coupled through the feedback transformer into the control section of the converter varying the pulse width of the square wave signal driving the MOSFETs, narrowing the pulse width if the output voltage is too high and widening it if it is too low. These pulse width variations provide the necessary corrections to regulate the magnitude of output voltage within its' specified limits.

Because the primary portion of the circuit is coupled to the secondary side with magnetic elements, full isolation from input to output is maintained.

Although incorporating several sophisticated and useful ancillary features, basic operation of the AFL270XXD series can be initiated by simply applying an input voltage to pins 1 and 2 and connecting the appropriate loads between pins 7, 8, and 9. Of course, operation of any converter with high power density should not be attempted before secure attachment to an appropriate heat dissipator. (See Thermal Considerations, page 13)

4.0 Inhibit Converter Output (Enable)

As an alternative to application and removal of the DC voltage to the input, the user can control the converter output by providing TTL compatible, positive logic signals to either of two enable pins (pin 4 or 12). The distinction between these two signal ports is that enable 1 (pin 4) is referenced to the input return (pin 2) while enable 2 (pin 12) is referenced to the output return (pin 8). Thus, the user has access to an inhibit function on either side of the isolation barrier. Each port is internally pulled "high" so that when not used, an open connection on both enable pins permits normal converter operation. When their use is desired, a logical "low" on either port will shut the converter down.

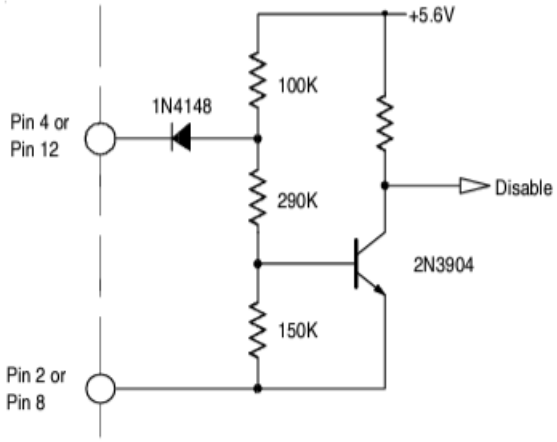

Figure 2. Enable Input Equivalent Circuit

Internally, these ports differ slightly in their function. In use, a low on Enable 1 completely shuts down all circuits in the converter, while a low on Enable 2 shuts down the secondary side while altering the controller duty cycle to near zero. Externally, the use of either port is transparent to the user save for minor differences in idle current. (See specification table).

5.0 Synchronization of Multiple Converters

When operating multiple converters, system requirements often dictate operation of the converters at a common frequency. To accommodate this requirement, the AFL series converters provide both a synchronization input and output.

The sync input port permits synchronization of an AFL converter to any compatible external frequency source operating between 500KHz and 700KHz. This input signal should be referenced to the input return and have a 10% to 90% duty cycle. Compatibility requires transition times less than100 ns, maximum low level of +0.8V and a minimum high level of +2.0V. The sync output of another converter which has been designated as the master oscillator provides a convenient frequency source for this mode of operation. When external synchronization is not required, the sync in pin should be left unconnected thereby permitting the converter to operate at its' own internally set frequency.

The sync output signal is a continuous pulse train set at 550 ± 50KHz, with a duty cycle of 15 ± 5.0%. This signal is referenced to the input return and has been tailored to be compatible with the AFL sync input port. Transition times are less than 100ns and the low-level output impedance is less than 50Ω. This signal is active when the DC input voltage is within the specified operating range and the converter is not inhibited. This output has adequate drive reserve to synchronize at least five additional converters. A typical synchronization connection option is illustrated in Figure 3.

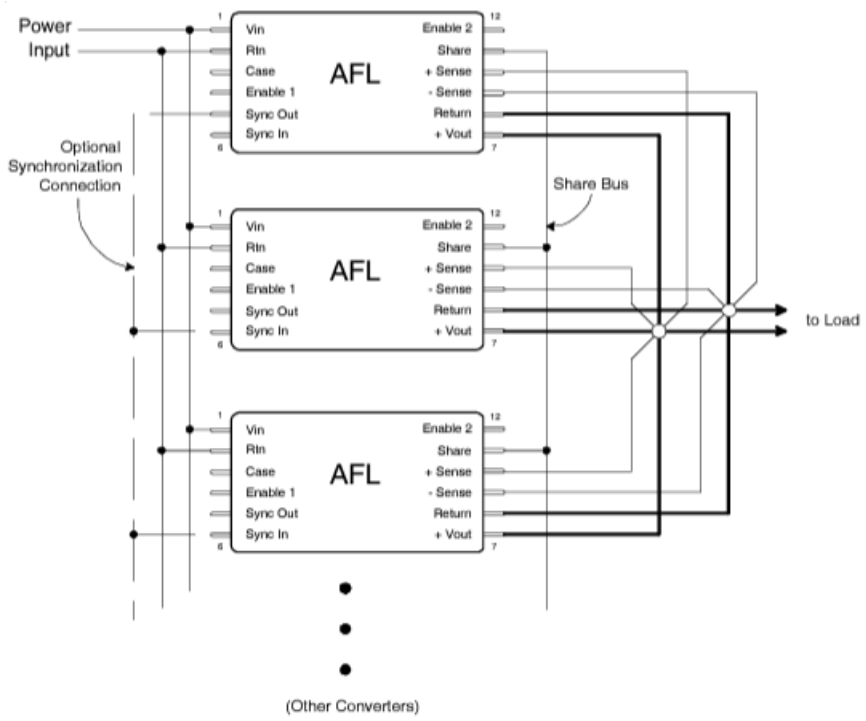

Figure 3. Preferred Connection for Parallel Operation

6.0 Parallel Operation-Current and Stress Sharing

Figure 3. illustrates the preferred connection scheme for operation of a set of AFL converters with outputs operating in parallel. Use of this connection permits equal current sharing among the members of a set whose load current exceeds the capacity of an individual AFL. An important feature of the AFL series operating in the parallel mode is that in addition to sharing the current, the stress induced by temperature will also be shared. Thus, if one member of a paralleled set is operating at a higher case temperature, the current it provides to the load will be reduced as compensation for the temperature induced stress on that device.

When operating in the shared mode, it is important that symmetry of connection be maintained as an assurance of optimum load sharing performance. Thus, converter outputs should be connected to the load with equal lengths of wire of the same gauge and should be connected to a common physical point, preferably at the load along with the converter output and return leads. All converters in a paralleled set must have their share pins connected together. This arrangement is diagrammatically illustrated in Figure 3. showing the output and return pins connected at a star point which is located close as possible to the load.

As a consequence of the topology utilized in the current sharing circuit, the share pin may be used for other functions. In applications requiring only a single converter, the voltage appearing on the share pin may be used as a "total current monitor". The share pin open circuit voltage is nominally +1.00V at no load and increases linearly with increasing total output current to +2.20V at full load. Note that the current we refer to here is the total output current, that is, the sum of the positive and negative output currents.

7.0 Thermal Considerations

Because of the incorporation of many innovative technological concepts, the AFL series of converters is capable of providing very high output power from a package of very small volume. These magnitudes of power density can only be obtained by combining high circuit efficiency with effective methods of heat removal from the die junctions. This requirement has been effectively addressed inside the device; but when operating at maximum loads, a significant amount of heat will be generated and this heat must be conducted away from the case. To maintain the case temperature at or below the specified maximum of 125°C, this heat must be transferred by conduction to an appropriate heat dissipater held in intimate contact with the converter base-plate.

Because effectiveness of this heat transfer is dependent on the intimacy of the baseplate/heatsink interface, it is strongly recommended that a high thermal conductivity heat transference medium is inserted between the baseplate and heatsink. The material most frequently utilized at the factory during all testing and burn-in processes is sold under the trade name of Sil-Pad® 400[1]. This particular pro duct is an insulator but electrically conductive versions are also available. Use of these materials assures maximum surface contact with the heat dissipator thereby compensating or minor variations of either surface. While other available types of heat conductive materials and compounds may provide similar performance, these alternatives are often less convenient and are frequently messy to use.

[1]Sil-Pad is a registered Trade Mark of Bergquist, Minneapolis, MN.

A conservative aid to estimating the total heat sink surface area ($A_{HEAT\ SINK}$) required to set the maximum case temperature rise (ΔT) above ambient temperature is given by the following expression:

$$A_{HEATSINK} \approx \left\{\frac{\Delta T}{80P^{0.85}}\right\}^{-1.43} - 3.0$$

Where

ΔT = Case temperature rise above ambient

P = Device dissipation in Watts = $P_{OUT}\left\{\frac{1}{Eff} - 1\right\}$

As an example, it is desired to maintain the case temperature of an AFL5015D at ≤ +85°C while operating in an open area whose ambient temperature is held at a constant +25°C; then

$$\Delta T = 85 - 25 = 60°C$$

From the Specification Table, the worst-case full load efficiency for this device is 83% @ 100 watts: then the power dissipation at full load is given by

$$P = 100 \cdot \left\{\frac{1}{.83} - 1\right\} = 100 \cdot (0.205) = 20.5W$$

And the required heat sink area is

$$A_{HEATSINK} = \left\{\frac{60}{80 \cdot 20.5^{0.85}}\right\}^{-1.43} - 3.0 = 56.3in^2$$

Thus, a total heat sink surface area (including fins, if any) of 56 in^2 in this example, would limit case rise to 60°C above ambient. A flat aluminum plate, 0.25" thick and of approximate dimension 4" by 7" (28 in^2 per side) would suffice for this application in a still air environment. Note that to meet the criteria in this example, both sides of the plate require unrestricted exposure to the ambient air.

8.0 Input Filter

The AFL50XXD series converters incorporate a single stage LC input filter whose elements dominate the input load impedance characteristic during the turn-on. The input circuit is as shown in Figure4.

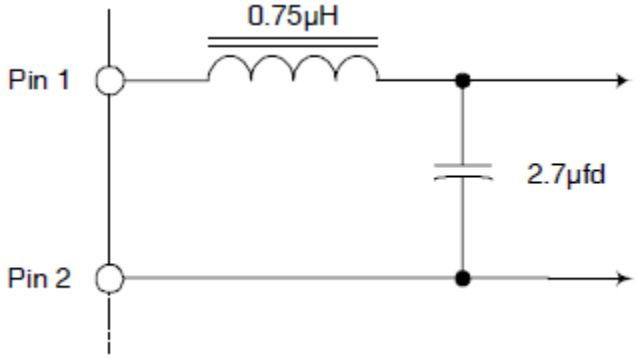

Figure 4. Input Filter Circuit

9.0 Undervoltage Lockout

A minimum voltage is required at the input of the converter to initiate operation. This voltage is set to 26.5 ± 1.5V. To preclude the possibility of noise or other variations at the input falsely initiating and halting converter operation, a hysteresis of approximately 2.0V is incorporated in this circuit. Thus, if the input voltage droops to 24.5 ± 1.5V, the converter will shut down and remain inoperative until the input voltage returns to ≈ 25V.

10.0 Output Voltage Adjust

By use of the trim pin (10), the magnitude of output voltages can be adjusted over a limited range in either a positive or negative direction. Connecting a resistor between the trim pin and either the output return or the positive output will raise or lower the magnitude of output voltages. The span of output voltage adjustment is restricted to the limits shown in Table 4.

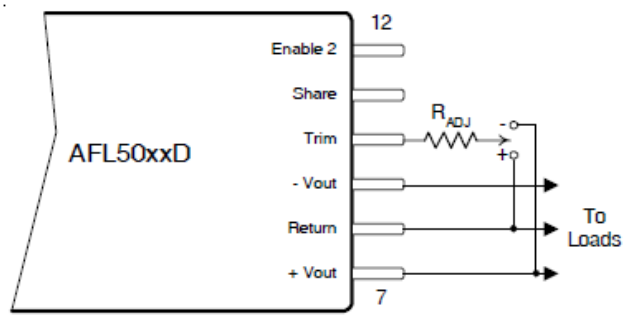

Figure 5. Connection for V_{OUT} Adjustment

Connect R_{adj} to + to increase, - to decrease

Table 4. Output Voltage Trim Values and Limits

AFL5005D		AFL5012D		AFL5015D	
V_{OUT}	R_{adj}	V_{OUT}	R_{adj}	V_{OUT}	R_{adj}
5.5	0	12.5	0	15.5	0
5.4	12.5K	12.4	47.5K	15.4	62.5K
5.3	33.3K	12.3	127K	15.3	167K
5.2	75K	12.2	285K	15.2	375K
5.1	200K	12.1	760K	15.1	1.0M
5.0	∞	12.0	∞	15.0	∞
4.9	190K	11.7	975K	14.6	1.2M
4.8	65K	11.3	288K	14.0	325K
4.7	23K	10.8	72.9K	13.5	117K
4.6	2.5K	10.6	29.9K	13.0	12.5K
4.583	0	10.417	0	12.917	0

Note that the nominal magnitude of output voltage resides in the middle of the table and the corresponding resistor value is set to ∞. To set the magnitude greater than nominal, the adjust resistor is connected to output return. To set the magnitude less than nominal, the adjust resistor is connected to the positive output. (Refer to Figure 5.)

For output voltage settings that are within the limits, but between those listed in Table 4, it is suggested that the resistor values be determined empirically by selection or by use of a variable resistor. The value thus determined can then be replaced with a good quality fixed resistor for permanent installation.

When use of this adjust feature is elected, the user should be aware that the temperature performance of the converter output voltage will be affected by the temperature performance of the resistor selected as the adjustment element and therefore, is advised to employ resistors with a tight temperature coefficient of resistance.

11.0 Mechanical Outlines

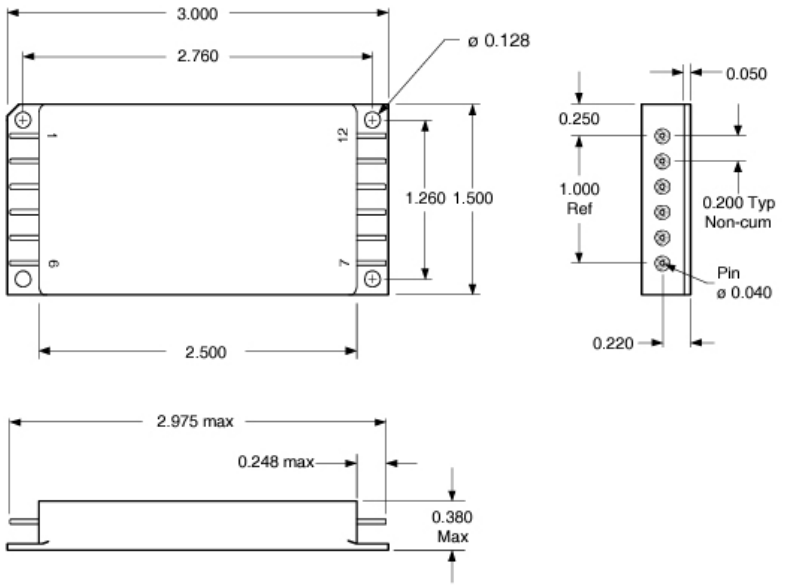

Figure 6. Case X

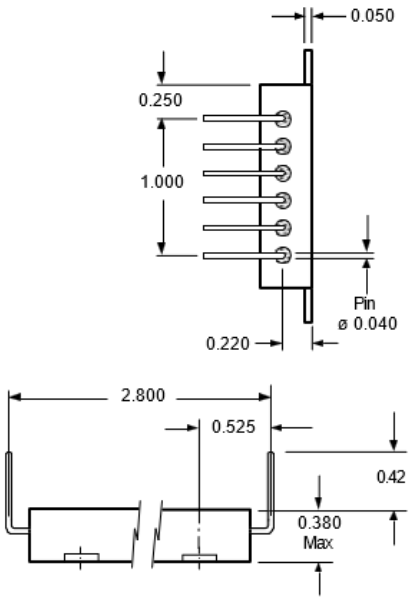

Figure 7. Case W

Pin Variation of Case Y

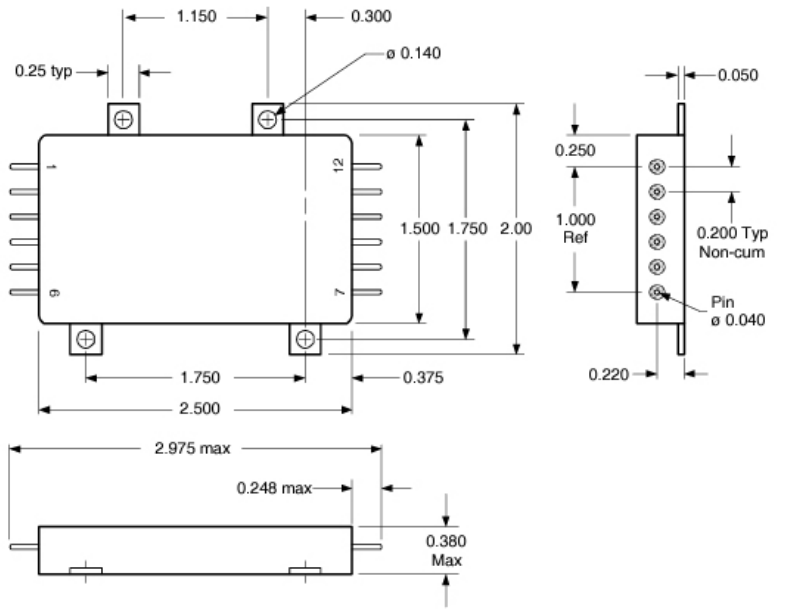

Figure 8. Case Y

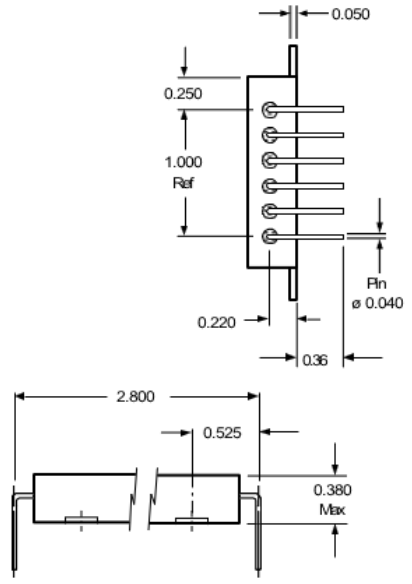

Figure 9. Case Z

Pin Variation of Case Y

Tolerances, unless otherwise specified: .XX = ±0.10

.XXX = ±0.005

BERYLLIA WARNING: These converters are hermetically sealed; however, they contain BeO substrates and should not be ground or subjected to any other operations including exposure to acids, which may produce Beryllium dust or fumes containing Beryllium

12.0 Pin Designation

Table 5. Pin Designation			
Pin #	**Designation**	**Pin #**	**Designation**
1	+ Input	7	+ Output
2	Input Return	8	Output Return
3	Case Ground	9	- Output
4	Enable 1	10	Output Voltage Trim
5	Sync Output	11	Share
6	Sync Input	12	Enable 2

13.0 Standard Microcircuit Drawing Equivalence

Table 6. SMD Equivalence	
SMD Number	**Part Number**
5962-02563	AFL5005D
5962-02564	AFL5012D
5962-02565	AFL5015D

14.0 Device Screening

Table 7. Device Screening					
Requirement	**MIL-STD-883 Method**	**No Suffix**	**ES – Note 2**	**HB**	**CH**
Temperature Range	–	-20°C to +85°C	-55°C to +125°C – Note 3	-55°C to +125°C	-55°C to +125°C
Element Evaluation	MIL-PRF-38534	N/A	N/A	N/A	Class H
Non-Destructive Bond Pull	2023	N/A	N/A	N/A	N/A
Internal Visual	2017	Note 1	Yes	Yes	Yes
Temperature Cycle	1010	N/A	Cond B	Cond C	Cond C
Constant Acceleration	2001, Y1 Axis	N/A	500Gs	3000Gs	3000Gs
PIND	2020	N/A	N/A	N/A	N/A
Burn-In	1015	N/A	48hrs at Hi Temp	160hrs at 125°C	160hrs at 125°C
Final Electrical (Group A)	MIL-PRF-38534 & Specification	25°C	25°C – Note 2	-55°C, +25°C, +125°C	-55°C, +25°C, +125°C
PDA	MIL-PRF-38534	N/A	N/A	N/A	10%
Seal, Fine and Gross	1014	Cond A	Cond A,C	Cond A,C	Cond A,C
Radiographic	2012	N/A	N/A	N/A	N/A
External Visual	2009	Note 1	Yes	Yes	Yes

Notes:

1. Best commercial practice
2. Sample tests at low and high temperature
3. -55°C to +105°C for AHE, ATO, ATW

15.0 Part Ordering