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Qualification Report

For

GaAs KS207 SPDT Switch In 3MM QFN Package

Prepared by

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AS9100
Registered

1. Scope

The qualification was performed to verify the reliability of 0.5um pHEMT process, the die, and it assembled in a lead-free 3mm 12-lead QFN surface mount hermetic package.

2. Reference Documents

2.1. MASW-011107 Preliminary Datasheet Revision V1
2.2. ANSI/ESDA/JEDEC JS-001 "For Electrostatic Discharge Sensitivity Testing Human Body Model (HBM) -Component Level"
2.3. ANSI/ESDA/JEDEC JS-002-2014 "For Electrostatic Discharge Sensitivity Testing Charged Device Model (CDM) – Device Level"
2.4. JESD22-A108 "Temperature, Bias, and Operating Life"
2.5. JESD47 "Stress-Test-Driven Qualification of Integrated Circuits"
2.6. J-STD-002 "Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires"
2.7. MIL-STD-883 "Department of Defense Test Method Standard, Microcircuit"
2.8. MIL-PRF-38535 "General Specification for Integrated Circuits Manufacturing"

3. Product Description and Information

The KS207 is a versatile, broadband, high isolation SPDT switch offered in a lead-free 3mm 12-lead QFN surface mount hermetic package. The design is based on the M/A-COM MASW-011107 MMIC which incorporates both series and shunt circuit elements with the locations optimized to achieve outstanding broadband performance to 15 GHz. The combination of broadband performance along with very fast switching and excellentsettling time make this device ideal for many applications, including Test & Measurement, EW and broadband communication systems.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using a pHEMT process.

3.1 Die Information

Die Size:	1.65 x 1.47 mm
Die Thickness:	4 mil
Fabrication Process:	0.5 µm pHEMT (IS)
Mask ID:	2127

4. Product Qualification Requirements

Qualification testing has been performed to validate the reliable operation of the MMIC die manufactured using a 0.5um pHEMT process. Tests are included to specifically address failure mechanisms related to elevated temperature, temperature cycling, and applied electrical bias.

4.1 General Information

Qualification Vehicle: MASW-011107

Qualification Tests

Test	Conditions	Endpoints	Fails/SS	Result
High Temperature Operating Life (HTOL) (JESD22-A108)	115°C Ambient Temperature Vcc = 5V	1000 Hours	0/234	PASS
Temperature Cycling (JESD22-A104)	Preconditioned Condition C -65°C to +150°C	500 Cycles	0/75	PASS
ESD (HBM)(JS-001)	1 positive discharge and 1 negative discharge per pinfor each pin combination	3 devices/level	0/3	250V Class 1A
ESD (CDM) (JS-002-2014)	1 positive discharge and 1 negative discharge; field induced	3 devices/level	0/3	1000V Class C3

* Not all parts subjected to Preconditioning were used for subsequent qualification testing.

5. Analysis of Results

5.1 High Temperature Operating Life (HTOL)

Description: This stress is used to identify any failure mechanisms accelerated by DC bias and elevated temperature that could occur during the lifetime of the product under test. Typical failure mechanisms that may occur include gate oxide breakdown, ionic contamination, and electromigration for silicon (Si) technologies, or gate sinking, ohmic contact degradation, and trap generation for gallium arsenide (GaAs) and gallium nitride (GaN) technologies. Process and/or assembly defects may be detected by this test in either technology. Devices are biased and operated at junction temperatures between 125°C and 160°C. Once failure mechanisms are identified, device lifetime at normal operating temperatures may be predicted. Devices are stressed for 1000 hours followed by electrical test. JESD22-A108 is used as a guideline.

Results: No evidence of wear out failure was found during this test. The HTOL test boards are optimized for stable use at elevated temperature. Since the boards are designed to withstand temperature extremes and not for optimal performance, the devices may not meet datasheet limits. Therefore, failure criteria is based on pre and post stress deltas. The results indicate that the devices are stable and reliable.

5.2 Electrostatic Discharge Sensitivity (ESD) Classification

Description: This stress is performed to evaluate the device's susceptibility to damage or degradation by electrostatic discharge that may be encountered during the routine handling and assembly of the device. Human Body Model (HBM) testing was performed per ANSI/ESDA/JEDEC JS-001 and Charged Device Model (CDM) testing was performed per ANSI/ESDA/JEDEC JS-002-2014.

Results The level of ESD that the device can safely tolerate was determined and recorded in the Qualification Tests table.

6. Predicted Failure Rates

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

$$AF_{(T_1 - T_2)} = e^{\frac{Ea}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

Where:

AF	=	acceleration factor
e	=	natural log
E_a	=	activation energy in electron volts
k	=	Boltzman's constant (8.62×10^{-5} eV/K)
T_1	=	derated temperature (K)
T_2	=	stress temperature (K)

The following assumptions have been made in the die manufacturer's determination offailure rates:

- Activation energy for the 0.5um pHEMT process = 1.88 eV
- Junction temperature during HTOL = 115°C

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

$$\text{Failure rate } (X^2) = \frac{X^2_{(2f+2,\alpha)}}{2*n*T*AF}$$

Where:

f	=	number of failures
α	=	1 – confidence level
n	=	quantity tested
T	=	test duration (hours)
AF	=	acceleration factor

Therefore, for the MASW-011107 built using 0.5 µm pHEMT (IS) process, the predicted failurerates are as follows:

Confidence Level	Use Temperature	X^2 Value	AF	Equivalent Device Hours	Failure Rate (FITS)	MTBF (Hours)
60%	85°C	1.83	111.28	2.60E+07	35.19	2.84E+07
60%	55°C	1.83	29319.90	6.86E+09	0.13	7.49E+09
90%	85°C	4.61	111.28	2.60E+07	88.43	1.13E+07
90%	55°C	4.61	29319.90	6.86E+09	0.34	2.98E+09

7. Screening

KCB has performed screening testing in accordance with MIL-PRF-38535 per the below table:

100% Screening	MIL-STD-883 Method/Requirement
Wafer lot acceptance test	5007
Nondestructive bond pull	2023
Internal visual	2010, test condition A
Pre-Cap Source Inspection	Per customer's PO
Temperature cycling	1010, test condition C: -65c to +150c 10 cycles
Constant acceleration	2001, test condition E (min) Y1 orientation only
Particle impact noise detection (PIND)	2020, test condition A
Serialization	See Internal Product Spec (IPS)
Radiographic	2012 two views
Pre burn-in electrical parameters	Per Table III Read and Record @ 25°C
Burn-in test	1015 240 hours at 125°C minimum Test Cond A, per burn-in configuration in Figure 1.
Post burn-in electrical	Per Table III Read and Record @ 25°C
Percent defective allowable (PDA) calculation	5 percent & 3 percent functional parameters at 25°C: PDA calculation include pre to post burn-in failure plus the delta calculation per table IV here-in.
Final electrical test	Per Table III Read and Record @ 0 and +85°C
Seal a. Fine b. Gross	1014
External visual	2009
Issue to QCI test sample selection	Group A, B, & D

The parts successfully completed screening, showing minimal variation through all screening steps. Test data and environmental test reports are available upon request.

8. Quality Conformance Inspection

KCB has performed quality conformance inspection in accordance with MIL-PRF-38535 Group B and D Testing per the below tables:

Group B for Class S Devices	**MIL-STD-883 Method/Requirement**
Subgroup 2	
a. Resistance to Solvents	2015 3(0)
b. Internal visual and mechanical	2013, 2014 2(0)
c. Bond strength	2011 Sample size = 4 parts, pull all wires, c = 0
(1) Thermocompression	1. Test condition C or D
d. Die shear	2019 or 2027 3(0)
Subgroup 3	Sample size = 3 parts all leads, c = 0
Solderability	2003 Solder temp 245°C±5°C
Subgroup 5	1005 Sample size = 10, c = 0
a. End-point electrical parameters	Per Table III Read and Record +25°C, 0 and +85C Note: Data collected at final electrical testing of main lot.
b. Steady state life	1005, Test condition D, 1000 hours, 125°C, per configuration in Figure 1
c. End-point electrical parameter	Per Table III Read and Record +25°C, 0 and +85c
Subgroup 6	Sample size = 15, c = 0
a. Temperature cycling	1010 Condition C, 100 cycles minimum
b. Constant acceleration	2001 Test condition E: Y1 orientation only
c. Seal (a) Fine (b) Gross	1014
d. End-point electrical parameters	Per Table III Read and Record +25°C, 0 and +85C

Group D	**MIL-STD-883 Method/Requirement**
Subgroup 1	
a. Physical dimensions	2016 Sample size = 15, c = 0
Subgroup 3	Sample size = 15, c = 0
a. Thermal shock	1011 Test condition B, 15 cycles minimum
b. Temperature cycling	1010 Test condition C, 100 cycles minimum.
c. Moisture resistance 6/	1004
d. Visual examination	In accordance with visual criteria of method 1004 and 1010
e. Seal (1) Fine (2) Gross	1014
f. End-point electrical parameters	Per Table III Read and Record +25°C
Subgroup 4	Sample size = 15, c = 0
a. Mechanical shock	2002 Test condition B minimum
b. Vibration, variable frequency	2007 Test condition A minimum
c. Constant acceleration	2001 Test condition E minimum, Y1orientation only
d. Seal (1) Fine (2) Gross	1014
e. Visual examination	In accordance with visual criteria of method 1004 and 1010
f. End-point electrical parameters	Per Table III Read and Record +25°C
Subgroup 5	Sample size = 15, c = 0
a. Salt atmosphere	1009 Test condition A minimum
b. Visual examination	in accordance with visual criteria of method 1009
c. Seal (1) Fine (2) Gross	1014
Subgroup 6	
a. Internal water-vapor content	1018 5,000 ppm max water content at 100°C 3(0) or 5(1)
Subgroup 9	Sample size = 3, c = 0 (minimum 3 leads/terminations)
a. Soldering heat	2036
b. Seal (1) Fine (2) Gross	1014
c. External Visual examination	2009
d. End-point electrical parameters	Per Table III Read and Record +25°C

The SPDT switch family completed all testing without incident. Electrical test results and environmental test reports are available upon request.